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Single Electron Transistor based Hardware designing of Linear Block Coding Technique for Error Correction in Digital Communication System

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Abstract

An increasing success in e-beam lithography technique revolutionized low power consuming, high integration density next generation nano device built consumer electronics. This has inspired Researchers to design several nanoscale devices such as Single Electron Transistor (SET) made Single Electron Devices (SED) that can be included in near future in every sphere of life. One such unique approach of the Researchers is to introduce SED in Digital Communication System. The major challenge faced by the Researchers is the unintentional error that often occurs in the receiver side of any Digital Communication System. It is essential to detect the error and correct it simultaneously during transmission. Several solutions have been reported so far in numerous research journals regarding this. Among other popular error correction techniques, the method opted here is Linear Block Coding Technique for error correction because of its unique feature of time consuming and efficient error detection process. Here the approach is to design a Single Electron Device based model of this error correction technique so that to incorporate it in near future for low power consuming Digital Communication System.

Keywords: Single Electron Transistor (SET), Single Electron Devices (SED), e-beam lithography, Linear Block Coding Technique, error correction technique, Digital Communication System.

Introduction

Low power consuming, high speed & high integration density SETs play a major role in modern nano scale electronics. SET based SEDs are one of the excellent examples of nano electronics technology. One single electron is suitable to accumulate one bit of information in the SET, this is why the Researchers emphasize most in manipulating electrons at a larger scale. In other words controlling the transport of an electron is Single Electron Transistor Technology. This fascinating technology showed enormous potential in the new physical effects of charge transport. Beside its innumerable benefits like – (a) simplicity of the device structures, (b) high integration density owing to its nano dimension, (c) high processing speed equal to electron speed, (d) low power consuming and (e) exquisite sensitivity which is about five orders of magnitude (is far better than conventional solid-state MOSFET transistors); SETs also have several open challenges waiting for elegant solutions. Thus SET is rising up to be indispensible in every sector of future electronic industry especially in digital electronics [1-12].

In Digital Communication System, a 'Linear code' is considered as one of the most efficient encoding and decoding algorithm. This technique is one of the easiest & simple techniques to detect and correct errors regarding its efficient algorithm. Extra parity bits used in this technique do not convey any information by themselves but using these extra parity bits it is possible to detect and correct errors in the received message. Thereby detecting and correcting the errors in the received message is sufficiently time consuming and much efficient. Moreover, Linear Block Codes has been extensively used in Digital Communication System where security and data integrity is of primary concern. Basically, the parity bits of linear block codes are linear combination of the message. Therefore, one can represent the encoder by a linear system described by matrices as shown in Fig.1 in the last section of this chapter.

Here, the aim is to realize SET based Linear Block coding technique and observe its performance to make it suitable for low power consuming next generation Digital Communication System.

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Linear block code error correction technique

Mathematical explanation

Using Parity Check code one can understand that error has occurred during the data transmission. But to know at which position the error has occurred Linear Block Coding technique is observed as better choice for serial data communication [13-17].

To transfer a 'k'-bit message further 'r'-bit is added making the total length of the message 'n'-bit (Fig.2), where k < n. The message block is denoted as D = [d_1 d_2 …….d_n] and the code word is likely to be C = [c_1 c_2 ……c_n]. Thus the total number of message is 2^k. Therefore, the possible code length for 2^k message is 2^n. Thus the valid message code length is ($2^n - 2^k$). In the Transmitter side (also called encoder section) to generate the code word we have C = DG; where G = Generator Matrix denoted by $[I_k: P]_{k\times n}$. The $I_k$is the Identity matrix of order 'k' and P denotes an arbitrary matrix of order [k × (n-k)] and $C = [D]_{1\times k} \times [G]_{k\times n}$. For example if the message bit length is k=4 and the total length of the coded message is n =7, then the valid message code length is (2^7 - 2^4). For any 4-bit message the code word can be derived from the Table- 1. Considering the Table-3.1 the code for message D_{13} is derived from D_{13} = [1 1 0 1] → C_{13} = D×G = [1 1 0 1 1 1 1]. The same code vector 'C' can also be achieved in the following way.

The Generator Matrix

$$G=\underbrace{\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&1&0\\0&0&0&1\end{bmatrix}}_{(I_k)}\underbrace{\begin{bmatrix}1&0&1\\0&1&1\\1&1&1\\0&0&1\end{bmatrix}}_{(P)} \quad \text{.....[1]}$$

$$C=[1\ 1\ 0\ 1]\ X\ \underbrace{\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&1&0\\0&0&0&1\end{bmatrix}}_{(I_k)}\underbrace{\begin{bmatrix}1&0&1\\0&1&1\\1&1&1\\0&0&1\end{bmatrix}}_{(P)}$$

= [1 1 0 1 111] .....[2]

Here the message [1 1 0 1] is multiplied with the Generator matrix and further it is XOR-ed. For detection and correction we use

$$R = C \oplus E \quad \text{.....[3]}$$

where E= Error Vector due to noise and R is message with error. Now let us consider that a noise has occurred within the communication channel that has changed the 3rd MSB. In other words, we can say that for the message [1 1 o 1], the Error Vector is calculated by XOR-ing the message with [0 0 1 0]; i.e., R= [1 1 0 1 1 1 1] ⊕ [0 0 1 0 0 0 0] = [1 1 1 1 1 1 1]; thus at the receiving end we get the error message which is the left most four bit, i.e., [1 1 1 1] instead of [1 1 0 1]. To detect the single bit error we perform the following calculations:-

$S = RH^T$ is the Error Syndrome. ……[4], where, H = $[P^T_{(n-k)\times k} : I_{(n-k)}]_{(n-k)\times n}$ …….[5]and H^T is the transposition of H Matrix. If S is [0 0 0] then the message has no errors, else if S has any non-zero value in the matrix then the message contains error. The position of the error bit can be found through the usual way as stated below.

R = C ⊕ E = [1 1 0 1, 1 1 1] ⊕ [0 0 1 0, 0 0 0]
= [1 1 1 1, 1 1 1]. ……..…..……[6]

$$H = [P^T : I_3] = \begin{bmatrix}1&0&1&0&1&0&0\\0&1&1&0&0&1&0\\1&1&1&1&0&0&1\end{bmatrix} \quad \text{…..……[7]}$$

$$H^T = \begin{bmatrix}1&0&1\\0&1&1\\1&1&1\\0&0&1\\1&0&0\\0&1&0\\0&0&1\end{bmatrix} \quad \text{……..[8]. Now}$$

$S = RH^T$

$$= [1\ 1\ 1\ 1,\ \ 1\ 1\ 1] \times \begin{bmatrix}1&0&1\\0&1&1\\1&1&1\\0&0&1\\1&0&0\\0&1&0\\0&0&1\end{bmatrix} = [1\ 1\ 1] \quad \text{……[9]}$$

The above calculations revealed that the error has occurred in the 3rd bit i.e., the 3rd MSB as presumed earlier. Thus one can easily detect the single error and correct the code using Linear Block Coding Technique. The same can be obtained for any size of messages.

Hardware realization using SET

At the transmitting end the block that is generating the particular code word for a given input message is code encoder shown in Fig.3. It consists of one Serial to Parallel Converter, one SRAM and one Parallel to Serial converter. Implementation of these circuits using SET has been shown consequently.

The Serial to Parallel converter is based on D Flip-Flops made from combination of AND gate and NOR gate. The Tunnel Junction based 2 input AND Gate, OR Gate and NOT Gate is designed in Fig.4, 5 and 6 respectively. Similarly the Tunnel

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Junction based NOR Gate and the D Flip-Flop are shown in Fig. 7 and Fig. 8 respectively. Comprising all, the Serial to Parallel converter is designed (Fig. 9). The '2 to 4' decoder (Fig. 10) is used to design a '4 to 16' decoder (Fig. 11). Using Fig. 11 and Fig.8 the SRAM is designed (Fig 12). The Parallel to Serial converter is used using same D Flip Flop (Fig. 13). A 3 input AND gate is shown in Fig 14. Whereas Fig 16, 17 and 18 shows tunnel junction based 2-bit counter, tunnel junction based 3-bit counter and tunnel junction based XOR Gate respectively. This is how the Transmitter is generating the particular code word. This code word is containing the actual message.

Similarly at the receiving end the circuitry that detects the error is shown in Fig 19, comprising of a Serial to Parallel Converter along with 7 AND Gates, T Flip-Flops, 2-bit Counter, 3-bit Counter, SRAM, XOR Gates designed using SET. The purpose of this circuitry is to detect error if any in the message and to correct it correspondingly and at the same time to make it low power consuming device. Most published research journals of Sarkar et.al demonstrate this novel approach in designing low power consuming nano electronic circuits for next generation operations [18-20].

The modus operandi of the proposed model

As stated earlier the code word is composed of the actual message and parity. Here we have shown example architecture with a 4-bit message; for this 4-bit total 16 messages (0000 to 1111) are available and correspondingly 16 code words are generated. The Table-1 at the last section shows code word for every message. In the code encoder circuitry the code word will be stored in the SRAM. As the number of code word is 16 so we need to take a 2^4 x 7 size of memory chip. The output of Serial to Parallel Converter is connected to the Address Bus of the SRAM. The messages are coming serially to the serial to parallel converter which is being fetched as parallel data by this converter and this data will be the address (message) of the SRAM, the stored data at each address i.e., the generated code will be sent to the Parallel to Serial Converter to make it serial data. Fig.3 shows a general architecture of this Code Encoder. The Data Write bus will be used to write the new code word to the SRAM when alterations are made in this circuitry.

Through the single channel the message within code word is coming serially to the error detection circuitry (Fig.19) where H SRAM (residing in the dashed block) will store the corresponding H matrix given in eq. [7]. Thereafter, eq.[8] will be calculated through the dotted block of the same said Fig.19. After 3 cycle of the 2-bit counter the output of the dotted block will be stored in the 3-bit serial to parallel converter i.e., the Error Syndrome (S). Now, eq. [8] will be loaded in H^T SRAM placed in solid block of Fig.19. If 3-bit Serial to Parallel Converter data is [0 0 0] then E_1 is 1 which signifies message is unaffected by noise. When noise arises within the input code word the serial to parallel converter data (S) will check with the H^T data which is stored in H^T SRAM as stated above and if a match is found, the 3-bit counter will stop corresponding to E=0. Now the matched position of the SRAM will signify the error position as shown in eq.[9] above.

Comparatavie analysis of the proposed model

The modelling of SET based Linear Block Coding Error Correction technique was largely tested on Monte Carlo based simulation settings for its maximum exploitation. The proposed modelling of this SET based system which has been configured as an IC considerably reduces power consumption and is efficient enough to detect the unwanted errors at a quicker speed. As a result, a very high-speed but accurate computation is indeed attained with this newly proposed SET IC design. The power dissipation for switching a single bit is reduced considerably as shown in the Table-2 below is of few µW which is absolutely low when compared to conventional CMOS devices. Accordingly, it shows tremendous prospect of providing much more component density thereby reducing the future IC sizes. Thus among all other merits of SET based ICs the model reflects its robustness than any conventional CMOS based circuit.

Table 2. Comparison table for CMOS and SET

Sl. No	Technology	Propagation Delay time / Gate	Faster times	Power dissipation / Gate	Consume Power
1	CMOS	12 ns	1	0.01 / 10-12 mW	1
2	SET	6 ns	2	~1µW	$1/10^3$

Conclusion

This SET device based Linear Block Code model efficiently detects error and consumes considerably less power compared to other existing error detection hardware models. Moreover, owing to its less complicated architecture the cost of the device can be quite low. Other concerned factors like time-

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delay, integration density, speed and robustness of the model is of far better standard when matched to present day CMOS-TTL logic circuits. With the steady increase in SET fabrication technology such type of model will be designed efficiently by the nano device engineers in near future. Thus this model can be considered as a successful competent in next generation Digital Communication System.

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Author Biblography

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Prof. Jayanta Gope, B.E., PhD (Nanotechnology) from Jadavpur Univ. India, is presently at CSET. His field of interest includes Nano device modeling, SET/ SED, Spintronic Devices, Hybrid CMOS-SET. He has several international publications in these field.

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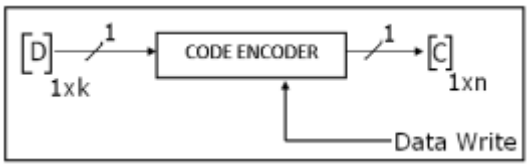

Fig.1 Linear Block Coding Technique Diagram

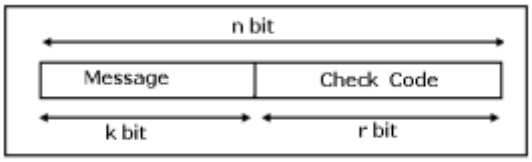

Fig.2 . Message bit length

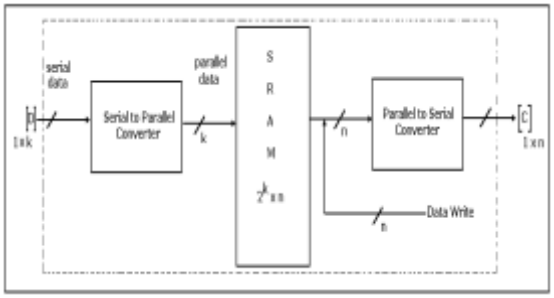

Fig.3 Code Encoder

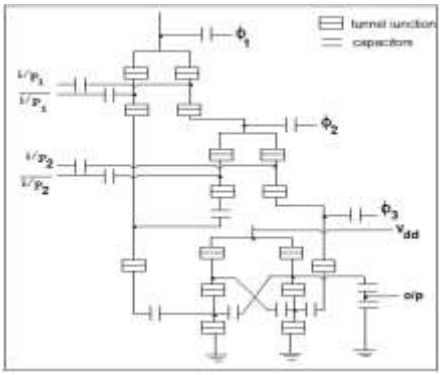

Fig.4 Tunnel Junction based 2 i/p AND Gate

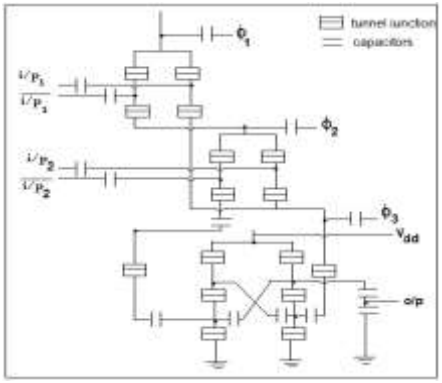

Fig.5 Tunnel Junction based 2 i/p OR Gate

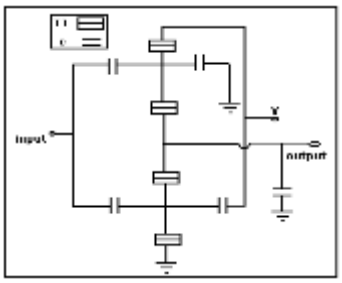

Fig.6 Tunnel Junction based 2 i/p NOT Gate

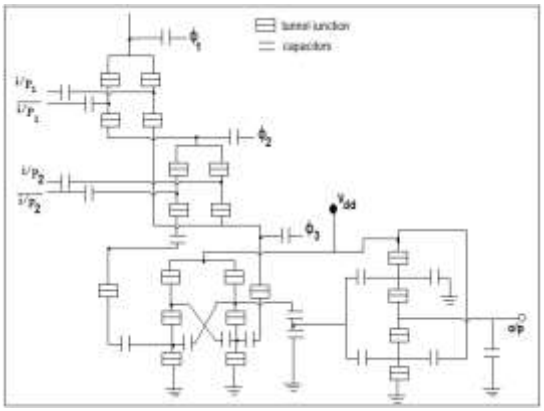

Fig.7 Tunnel Junction based 2 i/p NOR Gate

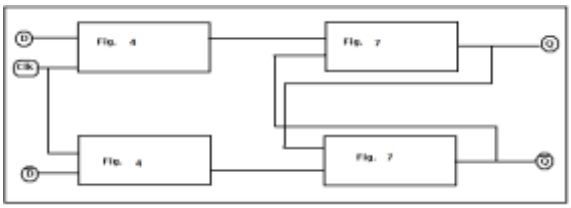

Fig.8 Tunnel Junction based DFlip Flop

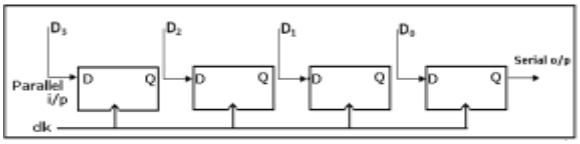

Fig.9 Tunnel Junction based 4 bit Parallel to Serial Converter

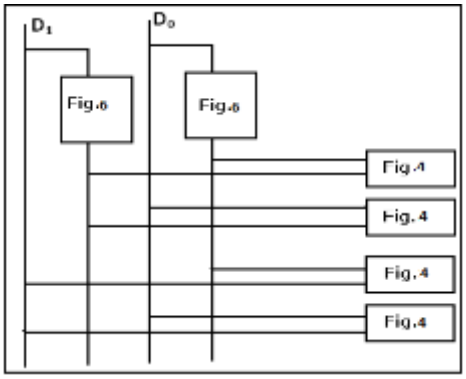

Fig.10 Tunnel Junction based 2^2 X 4 Decoder

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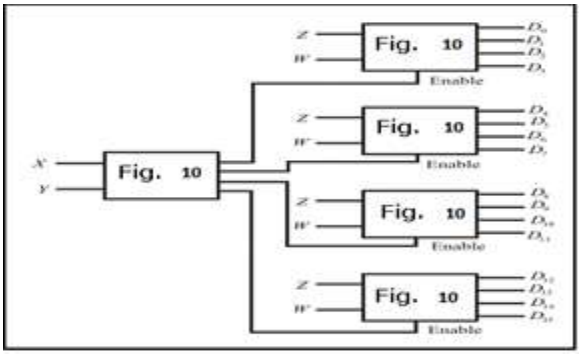

Fig.11 Tunnel Junction based 4 to 16 Decoder using 2 to 4 Decoder

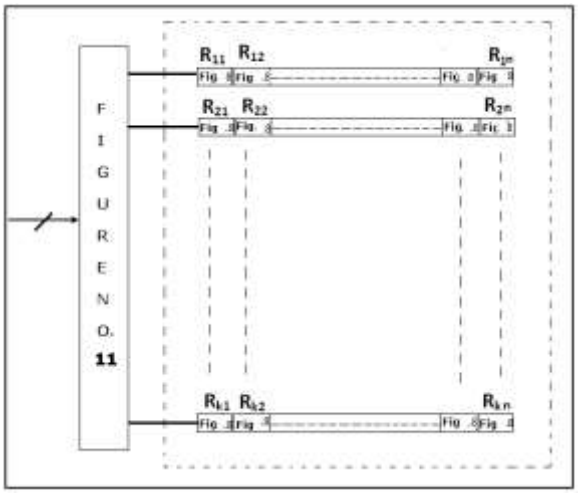

Fig.12 Tunnel Junction based SRAM 2^k X n

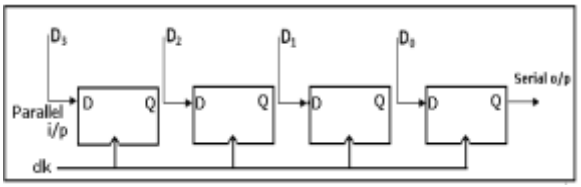

Fig.13 Tunnel Junction based Parallel to Serial Converter

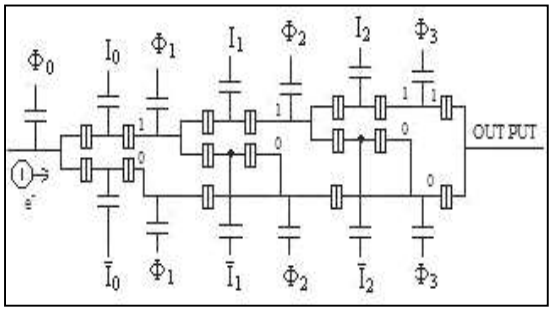

Fig.13 Tunnel Junction based 3 input AND Gate

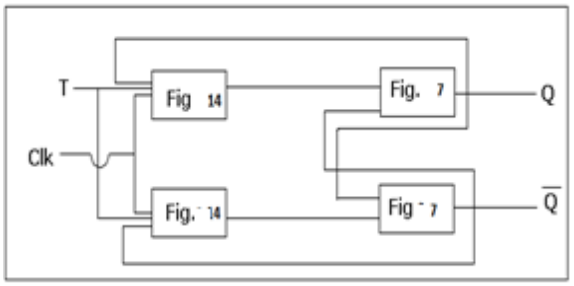

Fig.15 Tunnel Junction based T Flip-Flop

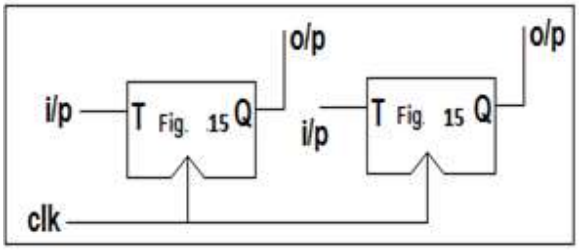

Fig.16 Tunnel Junction based 2-bit Counter

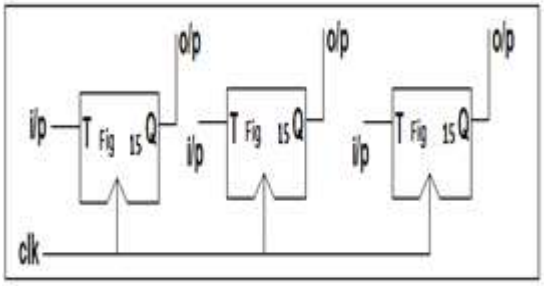

Fig. 17 Tunnel Junction based 3-bit Counter

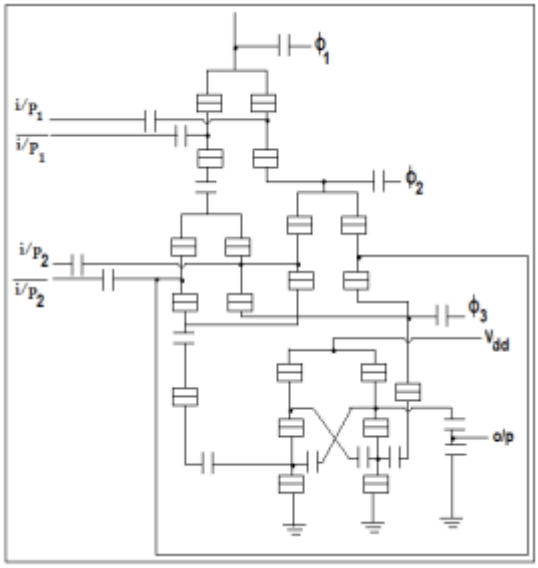

Fig. 18 Tunnel Junction based XOR Gate

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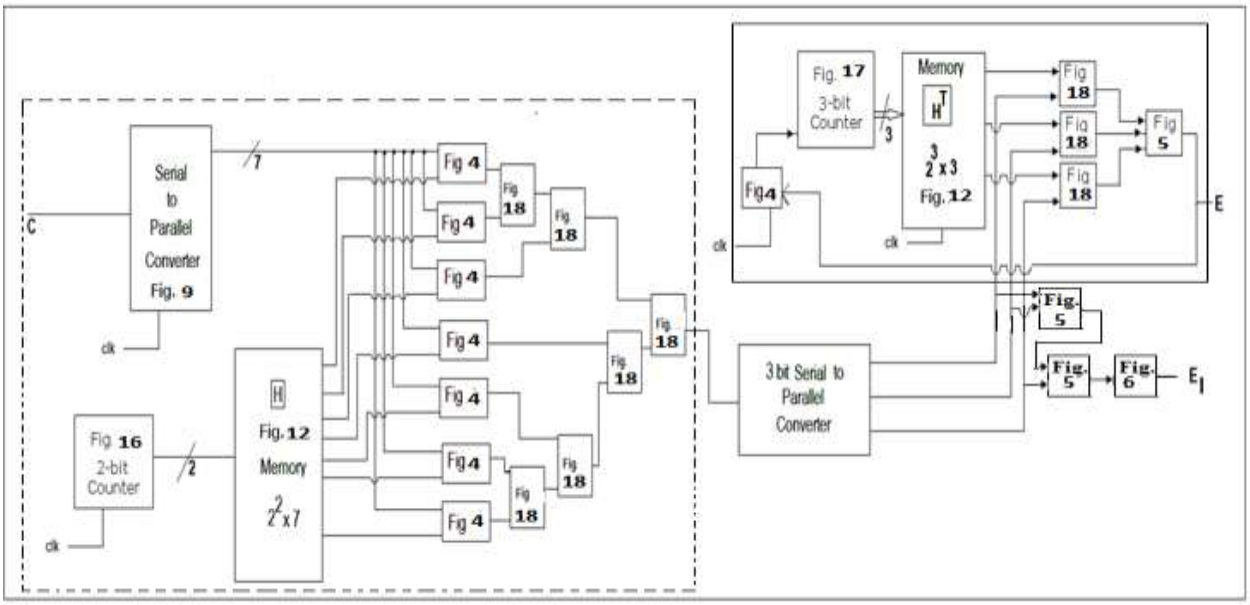

Fig.19 SET based Receiver of Linear Block Code Circuitry for Error Detection

Table- 1. Code word for any 4-bit message

[D] →	d_1	d_2	d_3	d_4	⇒	[C] →	c_6	c_5	c_4	c_3	c_2	c_1	c_0
D_0	0	0	0	0	⇒	C_0	0	0	0	0	0	0	0
D_1	0	0	0	1	⇒	C_1	0	0	0	1	0	0	1
D_2	0	0	1	0	⇒	C_2	0	0	1	0	1	1	1
D_3	0	0	1	1	⇒	C_3	0	0	1	1	1	1	0
D_4	0	1	0	0	⇒	C_4	0	1	0	0	0	1	1
D_5	0	1	0	1	⇒	C_5	0	1	0	1	0	1	0
D_6	0	1	1	0	⇒	C_6	0	1	1	0	1	0	0
D_7	0	1	1	1	⇒	C_7	0	1	1	1	1	0	1
D_8	1	0	0	0	⇒	C_8	1	0	0	0	1	0	1
D_9	1	0	0	1	⇒	C_9	1	0	0	1	1	0	0
D_{10}	1	0	1	0	⇒	C_{10}	1	0	1	0	0	1	0
D_{11}	1	0	1	1	⇒	C_{11}	1	0	1	1	0	1	1
D_{12}	1	1	0	0	⇒	C_{12}	1	1	0	0	1	1	0
D_{13}	1	1	0	1	⇒	C_{13}	1	1	0	1	1	1	1
D_{14}	1	1	1	0	⇒	C_{14}	1	1	1	0	0	0	1
D_{15}	1	1	1	1	⇒	C_{15}	1	1	1	1	0	0	1